What is claimed is:

1. A method for a computer system having a communication link processor and employing a FIFO buffer, comprising the steps of:

controling an asynchronous event storing and recording mechanism by discreet events into the FIFO at a location determined by a write pointer; and

causing an attached processor to read the recording mechanism's FIFO at a location determined by a read pointer;

said recording mechanism conditionally returning event and status information; and

conditionally incrementing the FIFO read pointer.

2. The method as recited in claim 1, wherein the fullness indication of the FIFO is returned in the read information as the value of the FIFO read pointer and write pointer.

3. The method as recited in claim 1, wherein the recording mechanism returns:

system status when the FIFO is completely empty; and

an event description when the FIFO has one or more valid entries.

4. The method as recited in claim 1, wherein the processor can instruct the recording mechanism to store multiple entries into the processor's main memory.

5. The method as recited in claim 4, wherein the said multiple storing of entries from the FIFO does not affect the state of the FIFO read pointer or write pointer.